Amendments to the Specification

Please replace paragraph [0042] with amended paragraph [0042] as follows:

[0042] Oxygen or fluorine ion implants (128) in the substrate (102) under each additional gate region (120) serve as gate oxide regions and reduce ~~reduces~~ gate leakage current and parasitic capacitance due to additional gate loading capacitance. Further, substrate (102) resistance is reduced under each additional gate region (120). Since only portions of the substrate (102) include the oxygen or fluorine ion implants (128), the oxygen or fluorine ion implants (128) are seen to be "discrete" implant regions that extend to the top surface (112) of the substrate (102) and form gate oxide regions in the substrate.

Please replace paragraph [0044] with amended paragraph [0044] as follows:

[0044] With reference to Fig. 2E, a thin gate oxide layer (132), or gate insulation layer, is applied or formed as a thin layer against the top surface (112). Fig. 2E illustrates that the thin gate oxide layer (132) is of uniform thickness. The gate oxide layer (132) covers the oxygen or fluorine implants (128), at the top surface (112), i.e., the thin gate oxide layer (132) does not encroach the oxygen or fluorine implants (128). The gate oxide layer (132) combines with the oxygen or fluorine ion implants (128), i.e., substrate gate oxide regions, to form ~~forms~~ a gate oxide on the substrate, with the gate oxide being thicker by having the oxygen or halogen ions providing gate oxide regions, i.e., oxygen or fluorine ion implants (128), in the substrate. In other words, the gate oxide consists of the gate oxide layer (132) and gate oxide regions, oxygen or fluorine ion implants (128). As such, the gate oxide is thicker in areas where the gate oxide layer (132) is formed over a discrete oxygen or fluorine ion implant (128) region than it is in areas where the gate oxide layer (132) does not cover a discrete oxygen or fluorine ion implant (128). Then a thick layer of gate electrode material, for example, a polysilicon layer (134) of polysilicon layer (134) is applied against the gate oxide layer (132). The polysilicon layer (134) is applied by deposition, for example. Selective

etching is performed to selectively remove the portions of the polysilicon layer (134), which forms the gate (118) and each additional gate region (120), as disclosed by Fig. 2F.